

IN THE CLAIMS

1 1. (Currently amended) A power management system for dynamically managing
2 power application to each of a plurality of devices in a computer system, ~~having one or more~~
3 ~~different components wherein power is dynamically supplied to each component~~, the power
4 management system comprising:

5 (a) a flexible clock generator circuit including at least one fixed rate clock
6 signal oscillator, said generator circuit for generating one or more ~~different~~ clock signals,
7 wherein the frequency of each of said signals can be in a range from less than to greater
8 than the frequency of said fixed rate clock signal; and ~~wherein each clock signal has a~~
9 ~~different predetermined frequency;~~

10 (b) a clock selector circuit responsive to a rate of usage of each of said
11 plurality of devices that directs a particular frequency of an output signal to be that, based
12 ~~on the task being performed by the computer system, dynamically adjusts the clock signal~~
13 supplied to each of said plurality of devices to maintain operation of each of said plurality
14 of devices and ~~each component of the computer system in order to reduce~~ minimize the
15 total power being consumed by the computer system.

1 2. (Currently amended) The system of Claim 1 further comprising a static power
2 management system ~~wherein power is withdrawn from components that are not currently active~~
3 ~~to reduce the power consumption of the computer system~~ for managing power application to
4 each of said plurality of devices by withdrawing power from a device that is not currently active,
5 and re-applying power when said device is needed to be active.

1 3. (Currently amended) The system of Claim 2, wherein the static power
2 management system includes ~~further comprises~~ a circuit for disconnecting the address, and
3 control data in and data out pins of a component of the computer system in order to reduce the
4 power consumption of the computer system.

1 4. (Currently amended) The system of Claim 1, wherein the clock generator circuit
2 includes ~~further comprises~~ a first oscillator that generates a first clock signal, a second clock
3 oscillator that generates a second clock signal, and a programmable clock circuit that generates a
4 third clock signal based on the second clock signal, ~~and a~~ wherein said clock select circuit ~~that~~
5 selects one of the first, second and third clock ~~signal~~ signals that is supplied to a portion of the
6 computer system to provide that portion of the computer system with a predetermined clock
7 signal.

1 5. (Currently amended) The system of Claim 4, wherein the clock select circuit
2 includes ~~further comprises~~ a clock state machine for determining the clock state of the computer
3 system at a predetermined time and a clock policy circuit for generating control signals to the
4 clock select circuit in order to output the appropriate clock signal.

1 6. (Currently amended) The system of Claim 5, wherein the clock state machine
2 provides ~~further comprises~~ an idle state ~~wherein~~ when the computer system is waiting for an
3 input, a busy state ~~wherein~~ when the computer system is performing a task, a sleep state ~~wherein~~
4 when the computer system has timed out due to inactivity and a dead state ~~wherein~~ when power
5 has failed to the computer system.

1 7. (Currently amended) The system of Claim 6, wherein the clock select circuit
2 includes ~~further comprises~~ a circuit that generates a system clock, a circuit that generates a
3 processor clock and a circuit that generates a co-processor clock wherein each of the clocks is
4 independently and simultaneously operable.

1 8. (Currently amended) The system of Claim 6, wherein, during the idle state, the
2 clock select circuit generates no clock for the phase locked loop and co-processor so that they are
3 off, the clock select circuit generates the first clock signal for the processor so that the processor
4 is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt
5 circuit so that the interrupt circuit is active and can increase the clock frequency for the computer
6 system ~~quickly~~.

1 9. (Original) The system of Claim 6, wherein, during the busy state, the clock select
2 circuit generates a high rate clock signal for the processor, the co-processor and the interrupt
3 circuits.

1 10. (Original) The system of Claim 6, wherein, during the sleep state, the clock select
2 circuit generates no clock signal for the processor and the co-processor.

1 11. (Original) The system of Claim 5, wherein the clock state machine is controlled
2 by an interrupt signal and software commands.

1 12. (Original) The system of Claim 4, wherein the programmable clock circuit
2 generates a fourth clock signal.

1 13. (Original) The system of Claim 12, wherein the first, second, third and fourth
2 clock signals have different frequencies.

1 14. (Currently amended) The system of Claim 13, wherein the first clock signal
2 frequency ~~is comprises~~ is 32 kHz, the second clock signal frequency ~~comprises is~~ is 24 MhZ, the
3 third clock signal frequency ~~comprises is~~ is 33 MhZ and the fourth clock signal frequency
4 ~~comprises is~~ is 66 MhZ.

1 15. (Currently amended) The system of Claim 4 further ~~comprises~~ comprising a time
2 of day circuit that generates time of day clock signals based on the first clock signal.

1 16. (Currently amended) The system of Claim 4, wherein the clock select circuit
2 ~~further comprises~~ includes means for dynamically changing the clock frequency applied to each
3 device ~~component~~ of the computer system based on the task being performed by the computer
4 system.

1 17. (Currently amended) The system of Claim 4, wherein the clock select circuit
2 ~~comprises~~ includes a multiplexer.

1 18. (Currently amended) The system of Claim 4, wherein the programmable clock
2 generator further ~~comprises~~ includes a prescalar unit and a post scalar unit whose outputs are fed
3 into a phase locked loop that generates a third clock signal and a fourth clock signal having
4 different frequencies.

1 19. (Currently amended) A power management method for a computer system
2 having ~~one or more different components~~ a plurality of devices wherein power is dynamically
3 supplied to each device component, the power management method comprising:

4 (a) ~~simultaneously generating by a clock generator having a crystal oscillator~~
5 one or more different clock signals wherein each clock signal has a different
6 predetermined frequency, and wherein said predetermined frequencies are selectable in a
7 frequency range from less than to greater than a frequency of said crystal oscillator; and

8 (b) dynamically adjusts adjusting the clock signal supplied to each
9 ~~component, device~~ of the computer system in order to reduce the total power being
10 consumed by the computer system.

1 20. (Currently amended) The method of Claim 19 further comprising ~~static power~~
2 ~~management method wherein power is withdrawn~~ withdrawing power from ~~components~~ devices
3 that are not currently active to reduce the power consumption of the computer system so as to
4 provide static power management method.

1 21. (Currently amended) The method of Claim 20, wherein said withdrawing power
2 includes the static power management further comprises disconnecting the an address, and
3 control data in and data out pins of a ~~component~~ device of the computer system method in order
4 to reduce the power consumption of the computer system method.

1 22. (Currently amended) The method of Claim 19, wherein ~~the clock generation~~
2 ~~further comprises~~ said generating further includes generating a first clock signal with a first
3 oscillator, generating a second clock signal using a second oscillator, generating a third clock

4 signal based on the second clock ~~signal~~ signals, and selecting by a programmable clock select
5 circuit one of the first, second and third clock signals that is supplied to a portion of the computer
6 system to provide that portion of the computer system with a predetermined clock signal.

1 23. (Currently amended) The method of Claim 22, wherein ~~the clock select further~~
2 ~~comprises~~ said selecting further includes determining by a state machine the clock state of the
3 computer system at a predetermined time and generating control signals to the clock select
4 circuit in order to output the appropriate clock signal.

1 24. (Currently amended) The method of Claim 23, wherein said selecting further
2 includes ~~the clock state machine further comprises~~ an idle state wherein the computer system
3 ~~method~~ is waiting for an input, a busy state wherein the computer system method is performing a
4 task, a sleep state wherein the computer system has timed out due to inactivity and a dead state
5 wherein power has failed to the computer system.

1 25. (Currently amended) The method of Claim 24, wherein said selecting further
2 includes ~~the clock select circuit further comprises~~ generating a system clock, generating a
3 processor clock and generating a co-processor clock wherein each of the clocks is independently
4 and simultaneously operable.

1 26. (Currently amended) The method of Claim 24, wherein during the idle state,
2 ~~generating~~ no clock signal is provided to ~~for~~ the phase locked loop and co-processor so that they
3 are off, and generating the first clock signal for the processor so that the processor is clocked at a
4 slow rate and generating a high rate clock for an interrupt circuit so that the interrupt circuit is
5 active and can increase the clock frequency for the computer system method ~~quickly~~.

1 27. (Currently amended) The method of Claim 24, wherein during the busy state,
2 ~~generating~~ a high rate clock signal is applied to ~~for~~ the processor, the co-processor and the
3 interrupt circuits.

1 28. (Currently amended) The method of Claim 24, wherein during the sleep state,
2 ~~generating~~ no clock signal is applied to ~~for~~ the processor and the co-processor.

1 29. (Original) The method of Claim 23, wherein the clock state machine is controlled
2 by an interrupt signal and software commands.

1 30. (Original) The method of Claim 22 further comprising generating a fourth clock
2 signal.

1 31. (Original) The method of Claim 30, wherein the first, second, third and fourth
2 clock signals have different frequencies.

1 32. (Currently amended) The method of Claim 31, wherein the first clock signal
2 frequency ~~comprises~~ is 32 kHz, the second clock signal frequency ~~comprises~~ is 24 MhZ, the
3 third clock signal frequency ~~comprises~~ is 33 MhZ and the fourth clock signal frequency
4 ~~comprises~~ is 66 MhZ.

1 33. (Currently amended) The method of Claim 22 further comprising generating
2 ~~comprises a time of day circuit that generates~~ time of day clock signals based on the first clock
3 signal.

1 34. (Currently amended) The method of Claim 22, wherein the clock select circuit
2 further ~~comprises~~ includes means for dynamically changing the clock frequency applied to each
3 device component of the computer system method based on the task being performed by the
4 computer system method.

1 35. (Currently amended) The method of Claim 22, wherein the clock select circuit
2 ~~comprises~~ includes a multiplexer.

1 36. (Currently amended) The method of Claim 22, wherein the programmable clock
2 circuit method further includes ~~comprises~~ a prescalar unit and a post scalar unit ~~whose~~ having
3 outputs that are fed into a phase locked loop that generates a third clock signal and a fourth clock
4 signal having different frequencies.

1 37. (Currently amended) A flexible clock generator, comprising:
2 a first oscillator that generates a first clock signal;
3 a second clock oscillator that generates a second clock signal;
4 a programmable clock circuit that generates a third clock signal based on the second
5 clock signal wherein a frequency of said third clock signal can be in a range from less than to
6 greater than a frequency of said second clock signal; and
7 a clock select circuit that selects one of the first, second and third clock signals ~~signal~~ that
8 is supplied to a portion of the computer system to provide that portion of the computer system
9 with a predetermined clock signal.

1 38. (Currently amended) The generator of Claim 37, wherein the clock select circuit
2 ~~further comprises~~ includes a clock state machine for determining the clock state of the computer
3 system at a predetermined time and a clock policy circuit for generating control signals to the
4 clock select circuit in order to output the appropriate clock signal.

1 39. (Currently amended) The generator of Claim 38, wherein the clock state machine
2 ~~further comprises~~ provides an idle state wherein the computer system is waiting for an input, a
3 busy state wherein the computer system is performing a task, a sleep state wherein the computer
4 system has timed out due to inactivity and a dead state wherein power has failed to the computer
5 system.

1 40. (Currently amended) The generator of Claim 39, wherein the clock select circuit
2 ~~further comprises~~ includes a circuit that generates a system clock, a circuit that generates a
3 processor clock and a circuit that generates a co-processor clock wherein each of the clocks is
4 independently and simultaneously operable.

1 41. (Currently amended) The generator of Claim 39, wherein, during the idle state,
2 the clock select circuit generates no clock for the phase locked loop and co-processor so that they
3 are off, the clock select circuit generates the first clock signal for the processor so that the
4 processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an
5 interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the
6 computer system quickly.

1 42. (Original) The generator of Claim 39, wherein, during the busy state, the clock
2 select circuit generates a high rate clock signal for the processor, the co-processor and the
3 interrupt circuits.

1 43. (Original) The generator of Claim 39, wherein, during the sleep state, the clock
2 select circuit generates no clock signal for the processor and the co-processor.

1 44. (Original) The generator of Claim 38, wherein the clock state machine is
2 controlled by an interrupt signal and software commands.

1 45. (Original) The generator of Claim 37, wherein the programmable clock circuit
2 generates a fourth clock signal.

1 46. (Original) The generator of Claim 45, wherein the first, second, third and fourth
2 clock signals have different frequencies.

1 47. (Currently amended) The generator of Claim 46, wherein a frequency of the first
2 clock signal ~~frequency comprises is~~ 32 kHz, a frequency of the second clock signal ~~frequency~~
3 ~~comprises is~~ 24 MhZ, a frequency of the third clock signal ~~frequency comprises is~~ 33 MhZ and a
4 frequency of the fourth clock signal ~~frequency comprises is~~ 66 MhZ.

1 48. (Currently amended) The generator of Claim 37 further ~~comprises~~ comprising a
2 time of day circuit that generates time of day clock signals based on the first clock signal.

1 49. (Currently amended) The generator of Claim 37, wherein the clock select circuit
2 ~~further comprises~~ includes means for dynamically changing the clock frequency applied to each
3 component of the computer system based on ~~the~~ a task being performed by the computer system.

1 50. (Currently amended) The generator of Claim 37, wherein the clock select circuit
2 ~~comprises~~ includes a multiplexer.

1 51. (Currently amended) The generator of Claim 37, wherein the programmable
2 clock generator ~~further comprises~~ includes a prescalar unit and a post scalar unit whose outputs
3 are fed into a phase locked loop that generates a third clock signal and a fourth clock signal
4 having different frequencies.

1 52. (New) A power management method for a computer system comprising:
2 dynamically managing power application to each of a plurality of devices of said
3 computer system including

4 a) first sensing a current operational usage of each said device; and
5 b) adjusting a frequency of a clock signal from a clock generator to each said device,
6 said frequency in proportion to said usage, wherein said clock signal is supplied by a flexible
7 clock generator including at least one oscillator, and wherein said generator can output at least
8 one signal having a frequency adjustable from less than to greater than a frequency of said at
9 least one oscillator.

1 53. (New) The method of Claim 52, further comprising:
2 statically managing power application to each said device including

- 3 a) second sensing to determine if a system device is being used;
4 b) withdrawing power including a clock signal from a device, if said device
5 is not being used;
6 c) determining if an unpowered device is needed; and
7 d) applying power including a clock signal to said unpowered device if said
8 device is needed.

1 54. (New) The method of Claim 53 further comprising:
2 optimizing by a device controller to manage said dynamic power application to each
3 device for a lowest computer system power consumption consistent with required operation of
4 each said device.

1 55. (New) The method of Claim 53 wherein said withdrawing power includes gating
2 off logic and a clock signal to a device, and applying power includes reapplying logic and a
3 clock signal to said device.